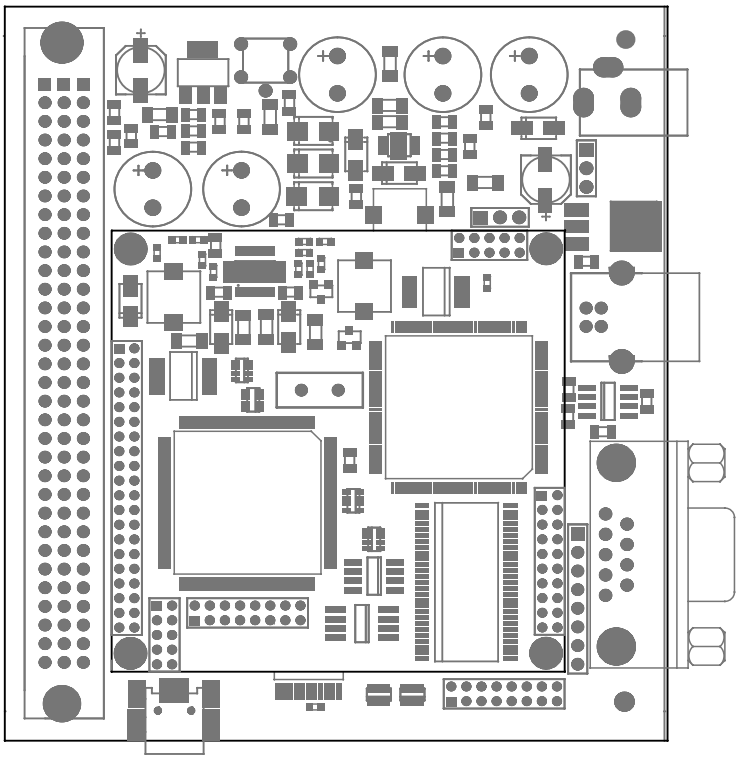
Danville Signal Processing, Inc.

ADDS-21261/Cyclone DSP & FPGA Evaluation Platform



User Manual

Version 1.00

Danville Signal Processing, Inc.

ADDS-21261/Cyclone DSP & FPGA Evaluation Platform (dspstak 21261zx – c96k46 System)

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This manual may contain errors, omissions or "typo's". Please send your comments, suggestions and corrections to:

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Introduction

Digital signal processing applications are one of the fastest growing areas in today's electronics field. It's not surprising that many different approaches can be used to address specific application requirements. DSPs and FPGAs are increasingly being combined to good effect in many very high performance signal processing targets. This platform demonstrates how a low cost 32 bit floating and fixed point DSP and a low cost FPGA can be integrated to form a powerful signal processing embedded application platform.

The Analog Devices' SHARC DSP is a 32 bit fixed and floating point programmable DSP. One of the major benefits of the SHARC is its inherent math precision and flexibility. For example, FFT algorithms are much easier to implement with a precision floating point DSP than with a fixed point processor. On the other hand, if you want to create a very high performance audio IIR filter, your best choice might be a fixed point implementation. With the SHARC, you choose the format that is most appropriate for your situation without incurring a performance hit since both of these formats are supported with one cycle instructions (actually two MACs per cycle for SIMD operations).

The ADSP-21261 is the lowest cost member of Analog Devices third generation SHARC family. This DSP offers a high level of integration including 1Mb of on-chip dual port SRAM, four high-speed serial ports and a SPI port. With its core running at 150 MHz (6.67ns instruction cycle time), the ADSP-21261 is capable of executing a complex 1024 point FFT in only 61us using SIMD instructions. Analog Devices has pin compatible parts with up to 3Mb of on-chip SRAM and core clocks of up to 333 MHz.

The Cyclone EP1C3 is the smallest member of Altera's FPGA line up. It includes 2910 logic elements (LEs). It also includes a PLL for clock multiplication, support for a variety of different I/O standards, on-chip SRAM blocks and a JTAG port. The FPGA is well suited for the consolidation of glue logic, peripheral expansion, signal processing acceleration and the integration of a microcontroller function.

As a symbiotic pair, the SHARC DSP and Cyclone FPGA are ideal for a variety of application areas including professional & consumer audio, voice recognition and noise reduction, software based radios, military applications, medical equipment, test instrumentation, communications products and modems.

In our platform, the DSP and FPGA are very closely coupled together so that both the DSP and FPGA can access resources such as external I/O and data converters, and perform tasks based largely on the needs of the application. Since both devices are user reprogrammable, the possibilities are very broad. Our platform uses the DSP for signal processing and control. The FPGA implements an SDRAM controller (64Mb SDRAM is included on our board), USB buffering and I/O expansion. The FPGA still has 85% of its resources free for other functions.

ADDS-21261/Cyclone Evaluation Platform

The ADDS-21261/Cyclone evaluation platform consists of products and tools provided by Danville Signal Processing, Analog Devices and Altera. The following items are included in the kit and discussed in later sections of this manual. Most of the components are discussed in detail in their own respective manual. Manuals are included in hard copy or on the ADDS-21261/Cyclone CD.

Hardware:

- dspstak 21261zx DSP Engine (includes dspblok 21261sm DSP Module)
- dspstak c96k46 I/O Module
- dspstak DSP & FPGA JTAG Adapter (includes extra 2mm & 0.100″ jumpers)
- 9 VDC Wall Adapter (North America 115V)

ADDS-21261/Cyclone CD

Tools:

- Analog Devices Visual DSP++ Version 4.0 (EZ-Kit Lite Version)
- Altera Quartus II Web Edition Software Suite
- Altera ByteBlaster II Parallel Port Download Cable

Cables:

- USB-A to USB-B Cable
- USB-A to USB-miniB Cable
- RS232 (DB9F to DB9M)
- 3.5mm Stereo Phono Jack / RCA Phono Y Cable (Qty 2)

Manuals:

- dspstak 21261zx User Manual
- dspstak c96k46 User Manual
- dspstak Family Users Manual
- ADDS-21261/Cyclone Evaluation Platform Manual (this manual)
- Analog Devices ADSP-2126x Core & Peripheral Manuals (ADDS-21261/Cyclone CD)
- Analog Devices AD1836A & ADSP-21261 Datasheets (ADDS-21261/Cyclone CD)
- Altera Cyclone Manual & EP1C3144 Datasheet (ADDS-21261/Cyclone CD)

Background

Danville Signal Processing, Analog Devices and Altera conceived the ADDS-21261/Cyclone Evaluation Platform. Each company contributed various resources to the project and each company had somewhat different objectives for participating. Arrow Electronics is our exclusive marketing partner for this platform. Many of the components used in the ADDS-21261/Cyclone platform can be purchased directly from Arrow Electronics.

Analog Devices & Altera

Analog Devices is a major supplier of DSP processors to the general-purpose market DSP market. Altera is a major supplier of FPGAs. Product managers at both companies recognized that their DSPs and FPGAs complemented each other for many applications, but that neither company had an evaluation platform that showcased this natural relationship. Furthermore, the majority of DSP-FPGA boards that exist in the general-purpose market are targeted for very demanding signal processing applications. These boards utilize state-of-the-art, high performance DSPs and FPGAs, but this performance comes at a corresponding cost.

The SHARC ADSP-21261 DSP and the Cyclone EP1C3 are not expensive devices. They both represent low cost choices that can be combined to address a tremendous number of signal processing challenges that are admittedly less demanding than your typical cell phone base station or MRI application. The ADDS-21261/Cyclone evaluation platform was conceived to demonstrate how these two technologies can be combined for general-purpose applications where cost considerations as well as performance requirements must be carefully considered. If you have not combined a DSP and an FPGA before, you may be surprised at the result.

Of course, from the Analog Devices and Altera perspective, they would like you to buy lots of parts. The ADDS-21261/Cyclone evaluation package is a vehicle that helps them get their message out.

Danville Signal Processing

Since the introduction of the Analog Devices third generation SHARC family, Danville Signal has been the leading supplier of general-purpose DSP boards based on the SHARC. Our dspstak 21262sx board was the first commercially available board based on this architecture. It was announced the same day that Analog Devices announced the ADSP-21262 in August 2003.

Danville's primary market is to provide DSP boards and modules to OEMs and systems integrators who typically require small and medium production volumes of 1 to 500 boards. If you need thousands of boards you will probably create and manufacture your own proprietary design.

You can learn more about our products at http://www.danvillesignal.com.

Danville Signal created and manufactures the ADDS-21261/Cyclone evaluation platform. It is based on our dspstak 21261zx DSP Engine and dspstak c96k46 I/O Module. These boards are discussed in detail in the dspstak manuals that are included with this platform and also later in this manual.

From a Danville Signal perspective, we hope that you will consider our boards if you have production requirements that can take advantage of our dspstak or dspblok product line. We also provide custom solutions where our standard products are not a good fit.

If you are creating your own design, you might consider our boards as prototype platforms for initial development. Our dspblok DSP modules are also available. They may be useful for integration into your larger design. For example, the dspblok 21261sm is the heart of the dspstak 21261zx. It includes the ADSP-21261, Cyclone EP1C3, SDRAM, core power supplies, flash and EE memory.

Arrow Electronics

Arrow Electronics is a leading electronic distributor. They sell both the Analog Devices and Altera components that are used in our boards. If you are going to create and manufacture your own design using ideas from this platform, we encourage you to contact your Arrow representative.

Arrow is offering this platform with special promotional pricing. Danville Signal, Analog Devices and Altera are subsidizing this package so that you can evaluate our products very inexpensively.

You can't buy production quantities of dspstak products from Arrow. If you are interested in using the dspstak or dspblok products for production, contact Danville Signal. Of course, Danville Signal is also an Arrow customer.

Introducing dspstak

DSP-based embedded applications often take the form of a digital signal processing engine coupled with a specialized data conversion and signal conditioning front end. The front end electronics and the DSP are almost always connected via high speed serial ports and the general purpose I/O ports of the DSP. In most cases, once the local memory and peripheral interfacing needs of the DSP are fulfilled, the DSP's data and address busses are no longer needed.

Standardized bus architectures such as PC/104, PCI and cPCI are all based on communicating via each board's data and address bus, while ignoring the needs of the most DSP / data conversion interfaces.

Danville's dspstak modules are designed to simplify DSP-based embedded applications. Generally, each dspstak consists of two modules: a DSP Engine, and a signal conditioning/data conversion I/O Module. The Interconnect Port consists of SPORTs (high speed serial ports), SPI, general I/O, clocks and power connections.

DSP Engine modules generally consist of a DSP processor, memory, power supplies and standard digital I/O such as RS-232 and USB. We currently have products based on Analog Devices' SHARC processors.

The I/O Modules may include signal conditioning electronics, A/D and/or D/A data converters, audio transceivers, unique connectors and a plethora of other special front end requirements. Since the I/O Module is separate from the DSP Engine Module, custom interfaces can be created quickly and inexpensively. Danville has a number of standard I/O Modules and often is willing to create a new one based on customer request. You can also create your own.

dspstak 21261zx DSP Engine

The dspstak™ 21261zx is a high performance digital signal processing engine based on the Analog Devices ADSP-21261 SHARC DSP and the Altera EP1C3 Cyclone FPGA.

The ADSP-21261 supports 32 bit fixed point and 32/40 bit floating point formats with SIMD instructions running at up to 150 MHz. This translates to a peak computation rate of 900 MFLOPS. The ADSP-21261 also includes very flexible peripherals including four independent serial ports (SPORTs) and a SPI port.

The Cyclone FPGA provides peripheral support including an SDRAM controller, SPI expansion and USB buffering. Chances are that you will never need to reprogram the FPGA even though it is completely reprogrammable. It could be used to complement the DSP with additional signal processing functions or you could use it to support special I/O requirements.

The heart of the dspstak 21261zx is Danville's dspblok 21261sm DSP Module. This module includes flash, SDRAM and EEProm memory in addition to the ADSP-21261 DSP and the Cyclone FPGA. The dspblok 21261sm is also available as a standalone module for integration into other boards.

The dspstak 21261zx is covered in detail in the dspstak 21261zx User Manual.

dspstak c96k46 I/O Module

The dspstak™ c96k46 is a multichannel audio ADC & DAC I/O module based on an Analog Devices' AD1836A audio sigma delta codec. Assuming a 12.288 MHz master clock, the AD1836A allows sampling rates of 96k, 48k, 32k, 24k and 16k with a resolution of 24bits. Other sampling rates are available by reprogramming the dspstak DSP Engine to another master clock frequency.

Industry standard, I2S interfacing is used to connect the AD1836A to the dspstak DSP Engine. Depending on the codec sample rate configuration, the AD1836A supports either two or four audio input channels and six audio output channels.

The dspstak c96k46 is covered in detail in the dspstak c96k46 User Manual.

dspstak & dspblok Family

Danville Signal offers many different dspstak DSP Engines and dspstak I/O Modules. Basic dspstak architecture is covered in the dspstak Family Users Manual.

Many of the DSP Engine options are variations of the dspstak 21261zx used in the ADDS-21261/Cyclone Evaluation Platform.

For example, the zx platform can use any of the pin compatible third generation SHARCs. These include the ADSP-21262 and ADSP-21364. SHARCs with special intellectual property, such as audio algorithms provided on on-chip ROM, can be accommodated after appropriate licensing arrangements have been established. Consult your Analog Devices representative if you are interested in these devices.

The dspstak 21261zx includes an EZ-Kit style debugger. This is a great feature for development, but an unnecessary expense for production units. We make versions with and without the on-board debugger.

You can find out more information on dspstak and dspblok products on our web site.

- http://www.danvillesignal.com/index.php?id=products_dspstak
- http://www.danvillesignal.com/index.php?id=products_dspblok

Technology

Danville Signal, Analog Devices and Altera each participated in the design of the dspstak 21261zx. Many of the design elements can be reused or modified for use in your own design. You can also modify the FPGA code for specific applications when using either the dspblok 21261sm or dspstak 21261zx.The following sections discuss some of these elements.

FPGA Configuration:

The FPGA is used for three functions in the dspstak 21261zx. These are SDRAM Controller, I/O and SPI expansion, and USB Buffering. These features use about 15% of the available resources of the FPGA. This leaves plenty of room for your own specific application.

The FPGA project used in the dspstak 21261zx is called zx. It was created as a combination of schematic entry using Quartus II version 4.1 SP2 and Verilog files. Open the zx project and open the zx.bdf file. The zx.bdf file is a schematic representing the top level of the whole project. The complete source is included on the ADDS-21261/Cyclone CD.

Altera provided the SDRAM controller design. It is written in Verilog and there is also a companion application note included on the CD. Danville Signal wrote the remaining functions. You may use them or modify them in your own designs. They were all created using the schematic entry method.

EZ-Kit Style Debugger:

Analog Devices has licensed their EZ-Kit style debugger for use on the ADSP-21261zx. This debugger works with VisualDSP++ with the same restrictions as an Analog Devices EZ-Kit. It also works with out restrictions with a full Visual DSP++ license. We do not provide schematics for the debugger, nor is it available for your own designs without an appropriate license agreement with Analog Devices.

Schematics:

Danville Signal provides complete schematics of the dspstak 21261zx, dspblok 21261sm and dspstak c96k46 on the ADDS-21261/Cyclone CD with the exception of the EZ-Kit style debugger. We expect that you will use these schematics to help you understand our design. They will also be useful if you are integrating the ADSP-21261 DSP and Cyclone EP1C3 FPGA in a custom design. Please review the proprietary technology section that follows on the next page.

Proprietary Technology:

Danville Signal owns the overall dspstak 21261zx, dspblok 21261sm and dspstak c96k46 designs. Analog Devices owns the EZ-Kit debugger portion of the design. The ADDS-21261/Cyclone Evaluation Platform is intended as both a demonstration and development platform. It is not our intent that you can clone it for your own purposes. We consider the following items proprietary to Danville Signal Processing, Inc.:

Danville Bootloader:

The Danville Bootloader is located in the flash memory and described in the dspstak 21261zx User Manual. It is used to store FPGA configuration and DSP application code and to boot the DSP after reset. You cannot duplicate this code without written permission from Danville Signal Processing, Inc.

Peripheral Microcontroller:

The Peripheral Microcontroller provides a variety of functions such as RS-232 support, I2C support, watchdog timer functions and bootloading functions. The DSP uses these features via API calls. We do not provide the source or object code for this device. The APIs are published in the dspstak 21261zx User Manual.

Board Layout, Schematics, etc:

The dspstak and dspblok family of products cannot be duplicated without the written consent of Danville Signal Processing, Inc. We will help you create your own compatible I/O Modules. If fact, we include some templates for this purpose on the CD.

DSP Source Code:

You can use all the source code provided on the CD as a starting point for your own application when you are using a dspstak or dspblok product as the target platform.

Although we consider all the source code provided on the CD as proprietary to Danville Signal Processing, Inc., you may use the code contained on the CD for your own applications on your own target with the exception of code contained in spi_21261zx.asm and pm_21261zx.asm, provided that you acknowledge our copyrights and don't resell the libraries or represent them as your own.

Disclaimer:

Danville Signal Processing, Inc. is making no claims or granting any permissions on behalf of Analog Devices Inc, or Altera Corporation.

Tools & Installation

Analog Devices and Altera have provided development tools in the ADDS-21261/Cyclone Evaluation Platform. CDs for these tools are included for your convenience. We suggest that you check each company's web site for updates or other licensing features. Of course, these tools are provided under terms set by their respective owners.

Analog Devices Visual DSP++:

The ADDS-21261/Cyclone Evaluation Platform is supported by Visual DSP++ Version 4.0. If you have an earlier version, you will need to update to this version or later.

There is an EZ-Kit license provided on the CD. This means that you can use Visual DSP++ for free with the same restrictions that you would have with an EZ-Kit. The main restriction is that program code is restricted to ¼ of the available memory after the first 90 days of use. You must have the dspstak 21261zx connected via its on-board debugger to use this license. The EZ-Kit license can be updated to a full Visual DSP++ license. Check with Analog Devices for specific details; we are making no claims on behalf of Analog Devices with regard to licensing.

If you are using an early version of Visual DSP++ Version 4.0, you will need to replace two of the dll files. The instructions and the necessary files are provided on the ADDS-21261/Cyclone CD in the VisualDSP_4_0_Additions directory.

Analog Devices ICE

The ADDS-21261/Cyclone Evaluation Platform includes a JTAG adapter that allows you to use an Analog Devices In Circuit Emulator (ICE) instead of the on-board debugger. If you are considering a higher performance emulator than the on-board debugger, we recommend the HPUSB ICE.

Altera Quartus II

Altera's Quartus II Web Edition supports the Cyclone EP1C3 FPGA. This version is may be used available for free under terms and conditions set by Altera Corporation. If you enable Quartus II to "phone home", you can also use a built in logic analyzer function called SignalTap II. We highly recommend this feature if you are modifying the default FPGA configuration. Altera also has other licensing options for Quartus II. You may wish to check to see which option is right for you.

Altera ByteBlaster II

Altera has provided a ByteBlaster II Download Cable with the ADDS-21261/Cyclone Evaluation Platform. This allows you to download FPGA configuration files via JTAG using the JTAG Adapter that is also supplied in the platform. The ByteBlaster is also used with SignalTap II for the logic analyzer function. The ByteBlaster is only used for development. The on-board serial flash normally uploads the FPGA configuration file via the Danville Bootloader.

TeraTerm Terminal Program

TeraTerm is a very useful freeware program that is distributed for your convenience on the CD. We use it in conjunction with the RS-232 and USB ports on the dspstak 21261zx. There are details on uploading DSP application code and FPGA configuration files in the dspstak 21261zx User Manual.

USB Device Drivers

The dspstak has two USB interfaces; the EZ-Kit style Debugger and a general purpose USB Port.

The debugger uses a USB mini-B connector. It is supported by Visual DSP++ Version 4.0. Start a new session and configure the debugger as an EZ KIT Lite (ADSP-21xxx) Visual DSP – Processor ADSP-21261.

The general purpose USB port requires device drivers that are located in the Danville\dspstak_usb_device_drivers directory on the ADDS-21261/Cyclone CD. This driver will cause the USB port to emulate a COM Port similar to RS-232 but much faster. If you are using TeraTerm you will probably need to reassign the USB Device to COM3 or COM4. It will probably initially assign COM5. The device driver works with Windows 2000 and Windows XP.

There is more information in the dspstak 21261zx User Manual.

Demonstrations & Setup

The ADDS-21261/Cyclone Evaluation Platform CD includes several software demos that illustrate many of the capabilities and features of the dspstak zx platform. While none of the examples are particularly sophisticated, we think that you will find them useful as take-off points for creating your own applications. We have tried to illustrate by example, most of the library functions that are included with the package.

Before you get started loading programs, your may want to connect your dspstak platform to your computer. We suggest the following steps:

- Connect either the RS-232 Serial or USB B Cable to your PC. You will want to install a terminal program such as the TeraTerm freeware program distributed on the CD.
- Connect a set of standard computer powered loudspeakers to any of the outputs using one of the 3.5mm/Phono Y cables.
- Connect a PC style microphone (or microphone headset) to the secondary audio inputs, J3. Install Shorting Jumpers on JH5 in positions 3&4. This will supply bias for an electret microphone.
- Connect a signal generator to the primary audio inputs, J2.
- Do not start VisualDSP yet.
- Plug in the coaxial power plug into the dspstak. If one of the demo programs is programmed into the flash, you will see the LEDs alternate on the I/O Module.

If you can restrain yourself, read the dspstak 21261zx and dspstak c96k46 User Manuals before going much further. The dspstak 21261zx User Manual explains how to upload programs to the flash memory.

You may also execute programs via the on-board debugger. Here are a few simple rules:

- Make sure that the dspstak is started before the debugger or an external emulator is connected and VisualDSP is started. This is necessary so that the Danville bootloader can load the FPGA code before the emulator or debugger takes charge.
- After VisualDSP is running with the debugger, you can press the RESET button on the dspstak 21261zx. The FPGA will not reset in this situation since you are on resetting the DSP in emulator mode.
- If you are running one of the sample programs and you don't see any text written to the terminal, you probably didn't reset the DSP after the emulator was connected.
- Make sure that you have loaded the two DLLs supplied on the ADDS-21261/Cyclone CD if you have an early version of VisualDSP 4.0. Instructions are on the CD.

Software Demos

There are five demonstration programs included on the CD. These programs are written in Analog Devices' SHARC assembly code. The SHARC assembly language is quite readable and easy to learn. For many users, the example programs will be very convenient to get you started on your own applications. If you haven't written any SHARC assembly before, we encourage you to examine the code carefully before you decide that everything should be coded in C.

Of course, you may still prefer to code some or all of your application in C. The SHARC architecture works well with C. VisualDSP provides a C compiler and libraries. Audio Devices' new VisualAudio graphical design tool supports the dspstak zx platform as well. You can find more information on our website: http://www.danvillesignal.com/index.php?id=zx_platform.

Here are brief descriptions of the demos. The programs share many of the same source files.

Hello World

Every platform needs a hello world program. This one just writes out a few messages to the RS-232 port and the USB port. It also blinks the LEDs on the c96k46 I/O Module. Hello World is a good way to learn how to read and write I/O. It does not rely on the dspstak c96k46 I/O Module. This makes it a good starting place if you are creating your own I/O Module.

SDRAM

This program is very similar to Hello World but it reads and writes all the SDRAM. It does not require the dspstak c96k46 I/O Module.

Talk-Thru

If every platform needs a hello world program, it also needs a talk-thru. Talk Thru demonstrates the dspstak c96k46 device driver.

The primary audio inputs, adc1 (J2) are looped back to two pairs of audio outputs, dac1 and dac2 (J4 & J5).

In a similar fashion, the secondary audio inputs, adc2 (J3) are looped back to the last pair of audio outputs, dac3 (J6). In this case there is +12dB of gain inserted in the signal path. This makes the secondary audio inputs more conducive for microphones.

FIR Filter

The FIR filter application takes the signal from the primary audio inputs (adc1) and splits this signal into a low pass section routed to dac1 and a high pass section routed to dac2. The corner frequency of both filters is 1 kHz. The filters were designed using the Parks-McClellan (Remez Exchange) method. They each have 127 taps and are linear phase.

The filters were implemented using SIMD instructions and floating point math.

The filter set is kind of an unoptimized speaker crossover network. You could build a very good optimized crossover network with this platform by choosing the filter and delay characteristics more carefully. You might want to sweep a sine generator through 1kHz to hear the result.

The secondary audio inputs, adc2 (J3) are just looped back to the dac3 audio output pair (+12dB gain).

Echo

The dspstak 21261zx has a lot of SDRAM available for creating large delay lines. In this application, we created a long stereo delay line using about 25% of the SDRAM. The input audio from adc2, is delayed about 5.5 seconds and fed into the dac3 audio output. We chose, adc2 since this input is configured for microphones. The sampling rate is set for 48kHz.

Long delay lines are very useful for implementing room correction algorithms, reverberation algorithms and many other audio effects. While a fixed delay is not going to realistically simulate the echo you might hear across a large canyon, we're sure you get the general idea.

The primary audio inputs, adc1 (J2) are just looped back to the dac1 and dac2 audio output pairs.

Other Resources

We encourage you to check the Danville web site for additional code, links and other resources. You can even contribute your own code to share with others. Send us an email if you are interested. Our developer's page is at http://www.danvillesignal.com/index.php?id=dspdev. You can email us at dsp@danvillesignal.com .

ADDS-21261/Cyclone Evaluation Platform CD

The following directories and files are contained on the CD:

Altera
- Cyclone
  - cyclone_device_handbook.pdf
  - cyclone_ep1c3144.pdf
- sdram_apnote
  - an334_adi_sdram-v1.2.pdf
- zx
  - // design files for the FPGA configuration

AnalogDevices
- 2126x Core Manual.pdf
- 2126x Peripheral Manuals.pdf
- AD1836A datasheet.pdf
- ADI Processors SelectionGuide.pdf
- ADSP-21261_anomalylist_072004.pdf
- ADSP-21261Datasheet.pdf

CY22393
- dspstak_zx.jed

Danville
- dspstak_usb_device_drivers
- IO_Module_PCB_Templates
- Manuals
  - dspstak_21261zx_user_manual_ver100.pdf
  - dspstak_c96k46_user_manual_ver100.pdf
  - dspstak_family_user_manual_ver200.pdf
  - ADDS-21261/Cyclone_Evaluation.pdf
- Schematics
  - dspblok_21261sm_sch.pdf
  - dspstak_21261zx_sch.pdf
  - dspstak_c96k46_sch.pdf

Software_Examples
- // hello world, talkthru, fir filter and echo

Tterm
- // Freeware terminal program

VisualDSP_4_0_Additions
- // Updated dll files for emulator and on-board debugger
- Installation.txt